Application No. 09/530,948
Reply to Office Action of August 13, 2003

<center>REMARKS/ARGUMENTS</center>

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-7 are pending in the present application. Claims 1-4 are amended and Claims 5-7 are added by the present amendment.

In the outstanding Office Action, Figures 1A and 1B were objected to. Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Claim 1 was rejected under 35 U.S.C. § 102(a) as unpatentable over Civanlar et al. (U.S. Patent No. 5,996,021, herein "Civanlar"). Claims 2-4 were indicated as allowable if rewritten in independent form.

Applicant thanks the Examiner for the indication of allowable subject matter. In light of this indication, new Claims 5-7 are added. In particular, new independent Claims 5 and 7 correspond to original dependent Claims 2 and 3, respectively, rewritten in independent form.

Regarding the objection to the drawings, substitute Figures 1A and 1B that have been modified in light of the comments noted in the outstanding Office Action are submitted herein. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the rejection of Claim 1 under 35 U.S.C. § 112, second paragraph, Claim 1 has been modified in light of the comments noted in the outstanding Office Action. Accordingly, it is respectfully requested this rejection be withdrawn.

Claim 1 was rejected under 35 U.S.C. § 102(a) as unpatentable over Civanlar. That rejection is respectfully traversed.

Independent Claim 1 is directed to a process for relaying IP frames as PDU application frames within an ATM switch with a distributed architecture and egress storage that includes a management module and plural ingress and egress junctors having a routing emulation function ensuring IP frame routing between users of ELAN media. Each of the ELAN media is represented by a router LEC module. The process includes offloading a frame relay function

<center>9</center>

into an ATM layer of the junctors by examining a first cell of each of the PDU application frames arriving at an ingress junctor to extract therefrom an IP address of a destination, by searching in a cache table of a junctor for a logical path and an outbound direction opposite a relevant IP address and opposite an ingress logical path and by using a translation obtained for all cells of the PDU application frames, and transmitting a request to update the cache table to the management module if the sought-after IP address is not located in the cache table. The cache table is updated by routing information originating from the routing emulation function residing in the management module

In a non-limiting example, Figures 4 and 3b that the frame relay function is offloaded into the ATM layer of junctors (7_i, 7_k and 7_j) that include cache tables (9_i, 9_k and 9_j) *within the ATM switch*. Cache tables (9_i, 9_k and 9_j) are updated by routing information originating from the routing emulation function residing in management module (4). This configuration allows for decentralization of the IP relay function (or IP forwarding) by limiting the role of the router (see also specification at page 11, lines 20-28).

Civanlar does not teach or suggest a frame relay function that is offloaded into the ATM layer of junctors that include cache tables within the ATM switch. Instead, Civanlar discloses a network protocol known as "Classical IP Over ATM" that has Address Resolution Protocol Servers (13, 16, 19 and 21) and routers (11, 14 and 17) that are wholly outside the ATM Switches (12, 15 and 18) (figure 1; and column 1, line 50 to column 2, line 44). The Address Resolution Protocol Server Servers (13, 16, 19 and 21) perform IP to ATM address translations outside ATM Switches (12, 15 and 18) (figure 1; and column 1, lines 63-66). Additionally, routers (11, 14 and 17) determines the next hop for transmission of a packet outside ATM Switches (12, 15 and 18) (figure 1; and column 2, lines 5-10). Thus, Cinvanlar does not disclose a frame relay function that is offloaded into the ATM layer of junctors. Further, Cinvanlar does not disclose junctors that include cache tables within the ATM switch.
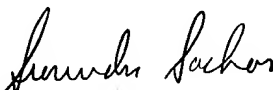
10

Thereby, independent Claim 1 and the claims depending therefrom patentably defines over <u>Civanlar</u>. Accordingly, it is respectfully requested this rejection be withdrawn.

In addition, as noted above, new independent Claims 5 and 7 are added in light of the indication of allowable subject matter in the outstanding Office Action. Applicants submit that the new claims are supported by the originally filed specification. The applied art do not teach or disclose a process for relaying IP frames as PDU application frames within an ATM switch that includes performing first and second translations. Further, the applied art do not teach or disclose a process for relaying IP frames as PDU application frames within an ATM switch that includes allocating in each of the egress junctors a queue for each of the first and second users, dynamically allocating internal indices and the egress queues in conjunction with updating of ingress translation caches, and using a mode for arbitration in PDU mode between the queues to ensure transmission of the cells without interleaving of the PDU application frames. Accordingly, it is respectfully submitted the new claims are allowable.

Consequently, in light of the above discussion and in view of the present amendment,

the present application is believed to be in condition for allowance. An early and favorable

action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Customer Number

22850

Tel: (703) 413-3000
Fax: (703) 413-2220
(OSMMN 08/03)

Gregory J. Maier
Attorney of Record
Registration No. 25,599
Surinder Sachar
Registration No. 34,423

GJM:SS:KLL:tdm
I:\ATTY\KLL\PROSECUTION\0154-2903-2PCT\01542903-AM 08-13-2003 OA.DOC